E2.02 Radiation-Tolerant Crew Laptop

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Texas State University - Radcat Sentinels

RadCat Sentinels

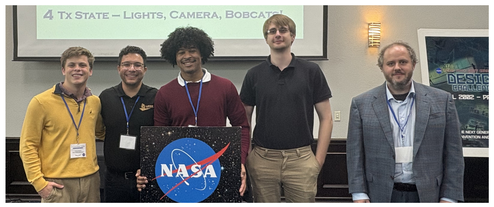

Fig. 1: Team Photo

Purpose and Importance

What Is Our Project About?

NASA is seeking a powerful, energy-efficient laptop capable of operating in the extreme conditions of cis-lunar travel for the upcoming Artemis missions. In this environment, digital electronics are exposed to ionizing radiation, which can permanently damage mission-critical components such as the processor. To address these challenges, the High-Performance Spaceflight Computing (HPSC) RISC-V processor, developed by Microchip, is being introduced as a radiation-tolerant solution. Our role is to design a crew laptop built around the HPSC processor while maintaining the form factor of the Framework 16 laptop.

Design Objective

- **Project Goal:** Define the high-level architecture for a radiation-tolerant crew laptop using the Framework 16 platform as a reference. This architecture definition encompasses the communication protocols, interfaces, and subsystem devices integrated into the overall design.

Design Features

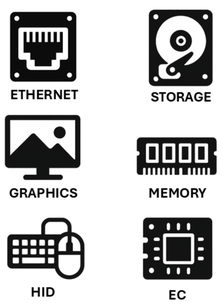

Fig. 2: Subsystems

High-Level Architecture Design

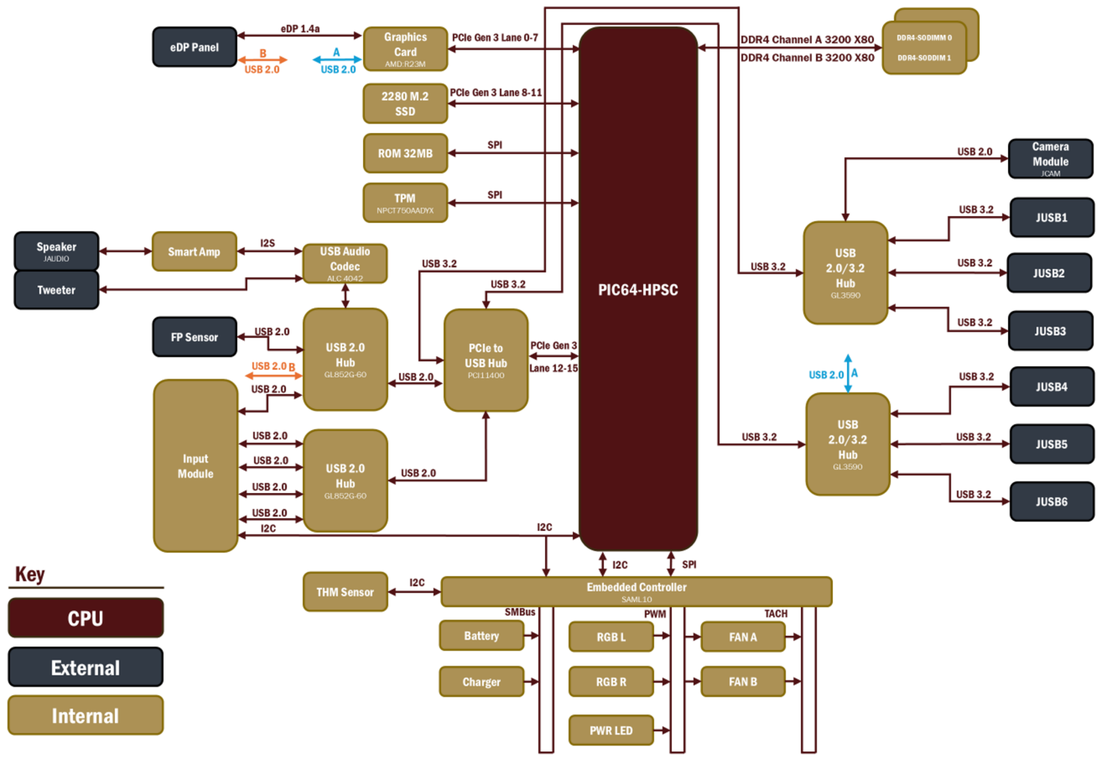

Fig. 3: High-Level Diagram

Radiation Threats to Hardware

- **Single Event Effects (SEE):** Change in electrical behavior of a semiconductor caused by a single high-energy particle striking the device, causing errors such as Single Event Upsets, Single Event Transients, Single Event Functional Interrupts, Single Event Latch-ups, Single Event Hard Errors, Single Event Gate Ruptures, and Single Event Burnouts.

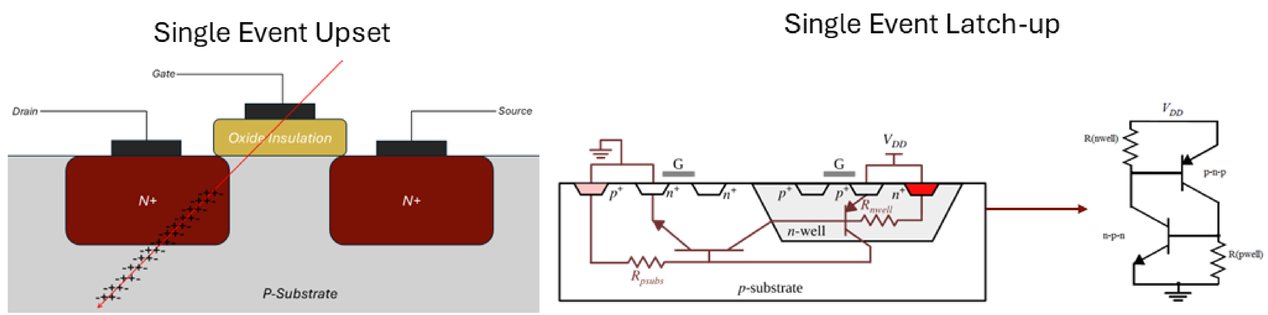

Fig. 4: Single-Event Upset

Future Development

Next Steps:

Future teams will be responsible for continuing the development of the HPSC-based Framework laptop. They will use the high-level architecture we defined to create a full schematic and fabricate the PCB. Once the hardware is built, the validation tools we developed will be used to verify the functionality of each subsystem and confirm the design meets project requirements.

Accomplishments

Spring 2025 Semester

- **Modified HSS Bootloader:** Customized the HSS bootloader to display our system's startup sequence over UART.
- **PolarFire SoC Research:** Researched the PolarFire SoC ecosystem, creating documentation for future
- **Bare-metal Example Testing:** Modified and deployed bare-metal firmware on the PolarFire Icicle Kit, using SoftConsole.

Fall 2025 Semester

- **NASA TSGC Conference:** Placed 2nd of 25 teams in the Fall 2025 NASA TSGC Design Challange.
- **High-Level Architecture Defined:** Developed the high-level system architecture for a radiation-tolerant crew laptop using the Framework 16 chassis and HPSC (RISC-V) processor, incorporating PCIe, USB, DDR4, and peripheral subsystems.
- **Solved the USB Interface Gap:** Identified a critical architectural limitation and engineered a working solution using the PCI11400 PCIe-to-USB host controller and the GL3590 multi-port USB 2.0/3.2 hub.

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