E1.01 Radiation-Tolerant Crew Laptop
USB Hub Development Board - Project Overview

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NASA Sponsor: Justin R. Bautista Faculty Advisor: Jeffery Stevens

Background

The space radiation environment disrupts electronic systems in three distinct ways:

- **Single Event Effects (SEEs):** Energetic, highly-charged particle strikes on semiconductors can cause bit flips, corrupting data, or damage devices via induced latchup or gate rupture.
- **Displacement Damage:** Heavy, high-energy particles can displace atoms within a semiconductor's lattice. Over time this results in performance degradation or device failure.
- **Ionization:** The removal of an atom's electrons by high-energy particles. This is especially harmful to insulators, like those found in FET gates, and will eventually lead to device failure.

These problems led NASA to partner with Microchip to develop the radiation-tolerant PIC64-HPSC. This processor will serve as the CPU for a modular system, dubbed the Radiation-Tolerant Crew Laptop, based on the Framework 16 Laptop.

Previous TXST Senior Design Teams developed a high-level preliminary system design and created a PCIe-to-USB Host Controller so the HPSC could serve as the CPU for a Framework 16 style system. Our mission is to create a USB Hub Development Board to test a viable architecture that meets the Framework 16 based system requirements.

Design Solution

To provide features commensurate with those on the Framework 16 Laptop, our development board offers:

× **8 Downstream Ports:**
- 3 Type-C USB 3.2 Gen 2 (10 Gbps)
- 5 Type-A USB 2.0 (480 Mbps)

× **2 Upstream Ports:**
- 1 Type-B USB 3.2 Gen 2 (10 Gbps)
- 1 Type-A USB 2.0 (480 Mbps)

USB Power Delivery Revision 3.1 with Extended Power Range:
- Power sinking up to 240W (48V @ 5A)
- Power supply up to ~50W (48V @ ~1A)

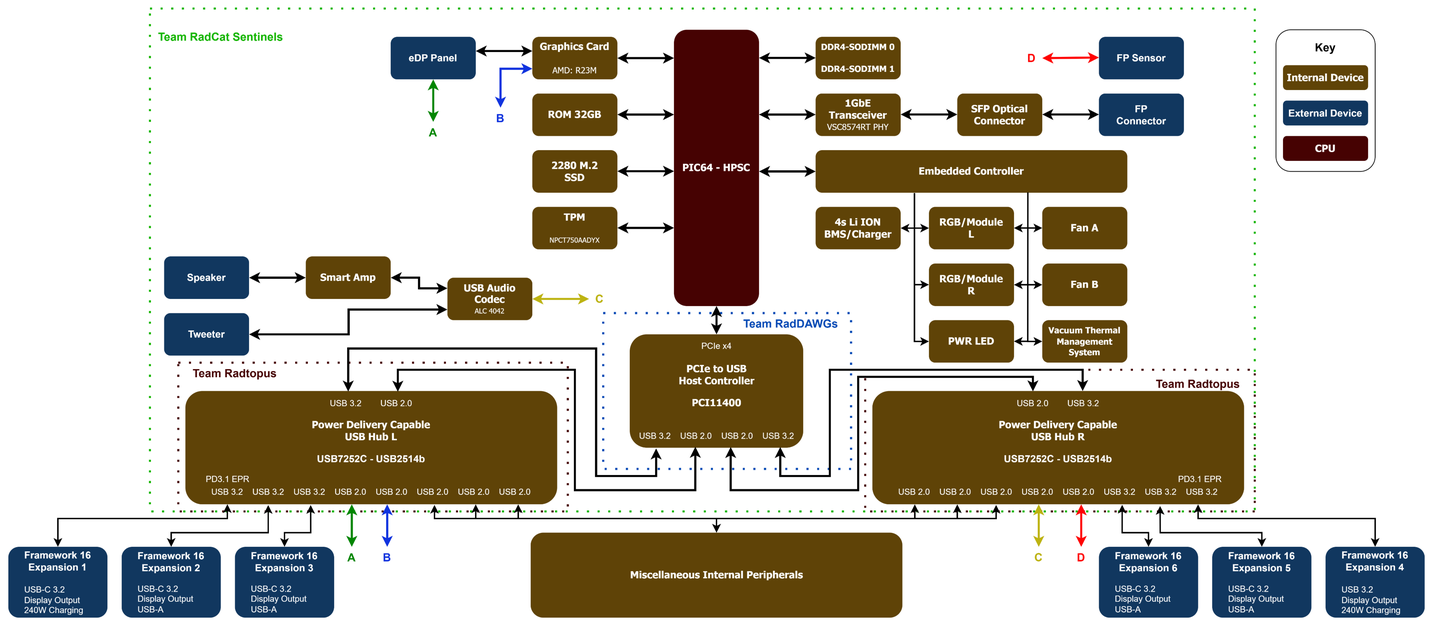
Dead Battery Support

Battery Charging Specification 1.2

Design Philosophy

- **Treat thermal performance as mission-critical** given the challenges of heat rejection in space and lunar environments.
- **Emphasize high-fidelity signal integrity** to ensure reliable high-speed communication in a radiation-affected environment.
- **Maintain an eye towards follow on development** by building in power connections for a follow-on 4s Li-ion Battery Management System/Charger.

Laptop Top Level Block Diagram



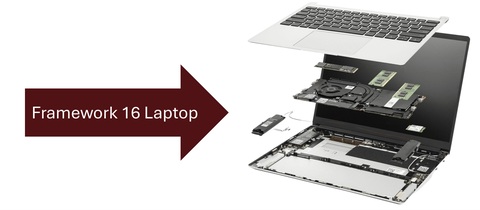
Project Schedule

Phase 1	Design Philosophy and Development Board Architecture Definition	Spring 2026
Phase 2	Development Board Schematic Creation	Spring 2026
Phase 3	PCB Layout	Fall 2026
Phase 4	Fabrication Prep and Release	Fall 2026
Phase 5	Development Board Validation and Testing	Fall 2026
Phase 6	Final Documentation Generation and Release	Fall 2026

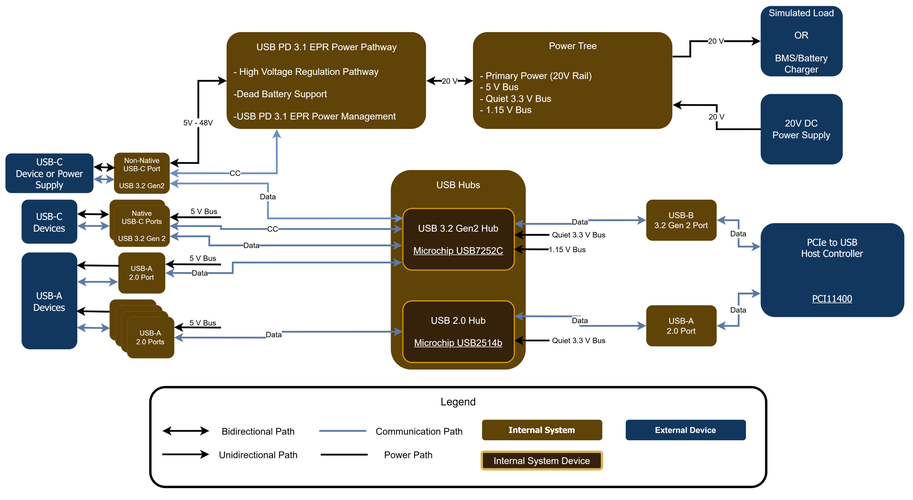
Accomplishments

Development Board Architecture Defined

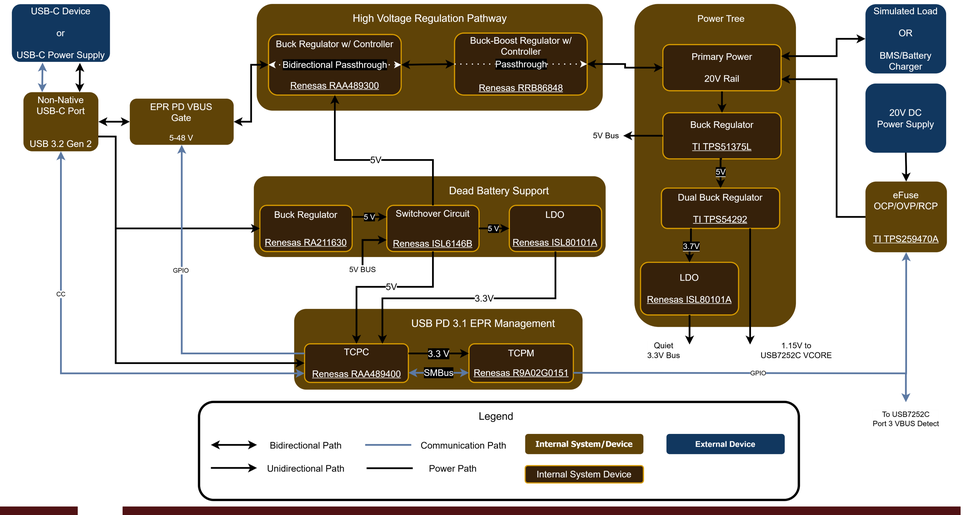
Schematic Creation: ~90% complete with the first draft of our schematics as of 23 April.



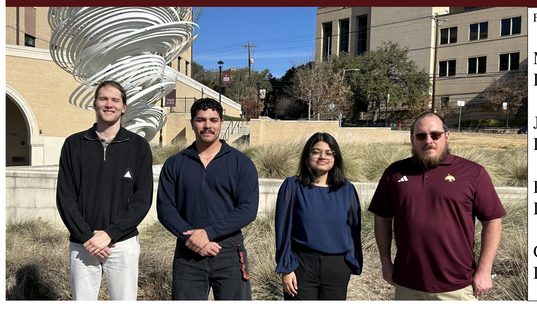
USB Hub Top Level Block Diagram



USB Hub Power Subsystem Block Diagram



Team



From left to right:

Matthew Giddens
Lead: High Speed Routing, PCB Layout

Javier Garcia
Lead: Power Delivery and Protection

Rabeea Fatima
Lead: Hub Configuration, Validation, Testing

Cameron Guillies – PM
Lead: System Integration, DFM, DFT

Acknowledgements

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Questions, comments and concerns regarding our project may be directed to Cameron Guillies

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